Ing-Chao (Richard) Lin

Dept. of Computer Science and Information Engineering
No. 1 University Rd., Tainan, Taiwan (ROC), 701
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EDUCATION

Ph.D.	Computer Science and Engineering, the Pennsylvania State University (PSU) Co-advised by Dr. Vijaykrishnan Narayanan and Mary Jane Irwin Dissertation: "System-level Power and Reliability Modeling"	Aug. 2002 – Aug. 2007
M.S.	Computer Science and Information Engineering National Taiwan University (NTU)	Sep. 1999 – Jun. 2001
B.Ed.	Information and Computer Education, National Taiwan Normal University (NTNU)	Sep. 1994 – Jun. 1997

PROFESSIONAL EXPERIENCE

Visiting Professor	Electrical and Computer Engineering, University of California, Santa Barbara (UCSB)	Aug. 2015 – Jul. 2016
Associate Professor	Computer Science and Information Engineering, NCKU	Feb. 2014 – present
Assistant Professor	Computer Science and Information Engineering, NCKU	Feb. 2009 – Jan. 2014
Research Assistant	Computer Science and Engineering, PSU	Jan. 2005 – Aug. 2006 Jan. 2004 – May 2004
Teaching Assistant	Computer Science and Engineering, PSU	Aug. 2003 – Dec. 2003

INDUSTRY EXPERIENCE

Staff R&D Engineer Real Intent Inc., Sunnyvale, California, USA — Oct. 2007 – Jan. 2009

- Designed frontend components for Synopsys Design Constraints parser to verify the correctness of set_false_path and set_multicycle_path commands by using the formal verification engines.
- Implemented Synopsys Design Constraints lint report function to automatically detect errors in SDC files and eliminate the errors.
- Implemented above components by using advanced and industrial-strength C++ programming techniques including design pattern and generic programming.
- Created significant test cases into the regression infrastructure to ensure and improve the quality of the products.

Co-Op IBM Electronic Design Automation Laboratory, Hudson Valley Research Park, New York — May 2004 – Nov. 2004

- Proposed a power estimation methodology for SystemC transaction-level models
- Implemented the methodology in IBM SystemC CoreConnect transaction-level models and

verified the methodology by comparing transaction-level and gate-level power estimations

SELECTED JOURNAL PUBLICATIONS

[J1] Ing-Chao Lin* and Jeng-Nian Chiou, "High-Endurance Hybrid Cache Design in CMP Architecture with Cache Partitioning and Access-Aware Policies", in IEEE Trans. on VLSI (TVLSI) System, vol. 23, no. 10, pp. 2149-2161, Oct. 2015 (SCI) (Top Journal in VLSI/EDA)

[J2] Ing-Chao Lin*, Yi-Ming Yang, and Cheng-Chien Lin, "High-Performance Low-Power Carry Speculative Addition with Variable Latency", in IEEE Trans. on VLSI (TVLSI) Systems, vol. 23, no. 9, pp. 1591-1603, Sept. 2015 (SCI) (Top Journal in VLSI/EDA)

[J3] Ing-Chao Lin*, Yu-Hung Cho, and Yi-Ming Yang, "Aging-Aware Reliable Multiplier with Adaptive Hold Logic", in IEEE Trans. on VLSI (TVLSI) Systems vol. 23, no. 3, pp. 544-556, March 2015(SCI) (Top Journal in VLSI/EDA)

[J4] Da-Wei Chang, Ing-Chao Lin*, Yu-Shiang Chien, Ching-Lun Lin, Alvin W. Y. Su, and Chung-Ping Young, "CASA: Contention-Aware Scratchpad Memory Allocation for Online Hybrid On-Chip Memory Management", in IEEE Trans. on Computer-Aided Design on Integrated Circuits (TCAD), vol. 33, pp. 1806-1817, Dec. 2014(SCI) (Top Journal in VLSI/EDA)

[J5] Kai-Chiang Wu, Ing-Chao Lin*, and Yao-Te Wang, "BTI-aware Sleep Transistor Sizing Algorithm for Reliable Power Gating Designs", in IEEE Trans. on Computer-Aided Design on Integrated Circuits (TCAD), vol. 33, no. 10, pp.1591-1595, Oct. 2014 (SCI) (Top Journal in VLSI/EDA)

[J6] Ing-Chao Lin*, Shun-Ming Syu, and Tsung-Yi Ho, "NBTI Tolerance and Leakage Reduction using Gate Sizing", in ACM Journal on Emerging Technologies in Computing Systems (JETC), vol. 11, no. 1, pp. 1-12, Sep. 2014 (SCI)

[J7] Ing-Chao Lin*, Kuan-Hui Li, Chia-Hao Lin, and Kai-Chiang Wu, "NBTI and Leakage Reduction Using ILP-based Approach" in IEEE Trans. on Very Large Scale Integration Systems (TVLSI), vol. 22, no. 9, pp. 2034-2038, Sep. 2014 (SCI) (Top Journal in VLSI/EDA)

[J8] Ing-Chao Lin*, Kuan-Hui Li, Chia-Hao Lin, and Kai-Chiang Wu, "NBTI and Leakage Reduction Using ILP-based Approach" in IEEE Trans. on Very Large Scale Integration Systems (TVLSI), vol. 22, no. 9, pp. 2034-2038, Sep. 2014 (SCI) (Top Journal in VLSI/EDA)

[J9] Ing-Chao Lin*, Kuan-Hui Li, Chia-Hao Lin, and Kai-Chiang Wu, "NBTI and Leakage Reduction Using ILP-based Approach" in IEEE Trans. on Very Large Scale Integration Systems (TVLSI), vol. 22, no. 9, pp. 2034-2038, Sep. 2014 (SCI) (Top Journal in VLSI/EDA)

SELECTED CONFERENCE PUBLICATIONS

[C1] Sheng-Wei Wang, Shuen-Shiang Yang and Ing-Chao Lin, “Improving Multicore System Reliability Using Online Cluster-based DVFS Technique,” in International Conference of Computer Aided-Design (ICCAD) Workshop on A Road for EDA Research in the Dark Silicon Era, Nov. 2014

[C2] C.-L. Lin, J.-W. Lin, B.-Y. Li, Y.-C. Lin, C.-C. Lin, Alvin W.-Y. Su, D.-W. Chang and I.-C. Lin, “An Novel On-Chip Memory Management Policy for Multicore System Platform

Supporting OpenCL," in International Conference of Computer Aided-Design (ICCAD) Workshop on Heterogeneous Computing Platforms, Nov. 2014

[C3] Ing-Chao Lin, Yao-Te Wang, Shuen-Shiang Yang, and Yi-Luen Wu, "Analyzing The BTI Effect on Multi-bit Retention Registers", in International Computer Symposium (ICS), pp. 250-259, Dec. 2014

[C4] Chia-Hao Lin and Ing-Chao Lin, "High Accuracy Approximate Multiplier With Error Correction", In Proceeding of International Computer on Computer Design (ICCD), pp. 33-38, Oct. 2013

[C5] Shun-Ming Syu, Yu-Hui Shao, and Ing-Chao Lin, "High-endurance Hybrid Cache Design in CMP Architecture with Cache Partitioning and Access-aware Policy", in Proceedings of Great Lakes Symposium on VLSI (GLSVLSI), pp. 19-24, May 2013

[C6] Yan-Han Lee, Ing-Chao Lin, and Shen-Wei Wang, "Impact of NBTI and PBTI effects on Ternary CAM", in Proceedings of International Symposium on Quality Electronics Design (ISQED), pp. 38-45, March 2013

[C7] Yu-Hung Cho, Ing-Chao Lin, and Yi-Ming Yang, "Aging-aware reliable multiplier design," in Proceedings of SOC Conference (SOCC), pp.322,327, 12-14 Sept. 2012

[C8] Chin-Hung Lin, Ing-Chao Lin and Kuan-Hui Li, "TG-based technique for NBTI degradation and leakage optimization," in Proceedings of International Symposium on Low Power Electronics and Design (ISLPED), pp.133,138, 1-3 Aug. 2011

[C9] Shi-Qun Zheng, Ing-Chao Lin, and Yen-Han Lee, "Analyzing throughput of power and thermal-constraint multicore processor under NBTI effect", in Proceedings of Great Lakes Symposium on VLSI (GLSVLSI'2011) pp. 415-418, 2011

[C10] Shi-Qun Zheng and Ing-Chao Lin, "Transaction-level error susceptibility for bus-based System-on-Chip: From single-bit to multi-bit," in Proceedings of International Computer Symposium (ICS), 2010 International , pp.670-675, 2010

[C11] Ing-Chao Lin, Suresh Srinivasan, Vijaykrishnan Narayanan, and Nagu Dhanwada, "Transaction Level Error Susceptibility Model for Bus Based SoC Architectures," in Proceeding of International Symposium on Quality Electronic Design, Mar. 2006 (ISQED '06)

[C12] Nagu Dhanwada, Ing-Chao Lin and Vijaykrishnan Narayanan, "A Power Estimation Methodology for SystemC Transaction Level Models," in Proceeding of International Conference on Hardware/Software Codesign and System Synthesis, Sep. 2005 (CODES+ISSS '05)

AWARDS AND HONORS

Excellent Young Electrical Engineer • Awarded by Chinese Institute of Electrical Engineering	2015
IEEE Senior Member	2014
NCKU Exceptional Performance Flexible Pay Award	2014
Best Paper Candidate, in VLSI/CAD Symposium	2013
Excellent Performance Award in Chiuan Yan Thesis competition	2012
Best Paper Candidate, in VLSI/CAD Symposium	2012
Best Advisor Award in the Computer Aided Design (CAD) contest	2012
Chair, IEEE Tainan Young Professionals	2011

AWARDS FOR EXCELLENCE IN SUPERVISION

Honorable Mention Award in Taiwan IEEE Best Ph.D. Thesis Award 2015
- Student Po-Hsun Wu

Silver Award in CAD Contest Problem E 2015
- Student Jian-Hong Lin and Yu-Wen Chen

Honorable Mention Award in CAD Contest Problem E 2015
- Student Jin-Yuan Lou

Honorable Mention Award in CAD Contest Problem D 2015
- Student Song-Yang Liao, Ting-Yan Lin, and En-Wei Zhang

Silver Award in Intelligent Electronics Contest 2015
- Yi-Chao Lin, Cheng-Chien Lin, Yi-shin Lu, Jin-Lun Lin

Best Master Thesis Award in IEEE Tainan Section Master Thesis Competition 2014
- Student Jeng-Nian Chiou

Gold Award in CAD Contest Problem E 2014
- Student Jian-Hong Lin and Yu-Wen Chen

Silver Award in CAD Contest Problem D 2014
- Student He-Teng Zhang and Jing-Pu Chen

Best Master Thesis Award in IEEE Tainan Section Master Thesis Competition 2013
- Student: Yi-Hua Li

Gold Award in Taiwan IEEE Master Thesis Competition 2013
- Student: Yi-Hua Li

Honorable Mention Award in IICM Master Thesis Competition 2013
- Student: Yao-Te Wang

Honorable Mention Award in IICM Master Thesis Competition 2013
- Student: Shun-Ming Syu

Gold Award in CAD Contest Problem A 2013
- Student He-Teng Zhang

Excellent Performance Award in IICM Master Thesis Competition 2012
- Student: Yu-hung Cho

Gold Award in CAD Contest Problem A 2012
Student He-Teng Zhang

Gold Award in Chiuan Yan Thesis competition 2012

FUNDED PROJECT

Hybrid DRAM Management (II) Dec. 2015 – Dec. 2016
- Supported by Industrial Technology Research Institute

Multicore System Design and On-chip Memory Management for Heterogeneous Computing May 2014 – Apr. 2016
- Supported by Ministry of Science and Technology, Taiwan

Hybrid DRAM Management (I) Jan. 2015 – Dec. 2015
- Supported by Industrial Technology Research Institute

Design of Reliable 3D Multicore Systems Aug. 2014 – Oct. 2015
- Supported by Ministry of Science and Technology, Taiwan

On-chip Memory Management in Multicore Systems with OpenCL Aug. 2013 – Nov. 2014
- Supported by Ministry of Science and Technology, Taiwan

Leakage and Aging co-optimization Aug. 2011 – Oct. 2012
- Supported by Ministry of Science and Technology, Taiwan

Aging Mitigation of SoC Bus Aug. 2010 – Jul. 2011
- Supported by Ministry of Science and Technology, Taiwan

Handling Soc Bus Degradation — Sep. 2009 – Nov. 2010
- Supported by Ministry of Science and Technology, Taiwan

COURSES TAUGHT

VLSI Design	Reliable Low Power System Design	VLSI Design Automation
Hardware and Software Codesign	Programming Languages	Computer Organization
Cyberphysical System	Network and Information Technology	Advanced Programming Technique

CERTIFICATES

Certificate of System-on-Chip Design — May 2006
- Issued by the Department of Computer Science and Engineering, PSU

Computer Science Teacher Certificate in Middle and High School Education — Jul. 1999
- Issued by the Ministries of Education, Taiwan

PROFFESIONAL SOCIETIES

Senior Member	Institute of Electrical and Electronics Engineers (IEEE)
Member	Association of Computing Machinery (ACM)
Life Member	Taiwan IC Design Society (TICD)
Life Member	Institute of Information and Computer Machinery (IICM)
Life Member	The Chinese Institute of Electrical Engineering
Life Member	Taiwan Institute of Electrical and Electronic Engineering
Member	Association of Computing Machinery (ACM) CS Society
Member	Association of Computing Machinery (ACM) DA Society
Member	IEEE Circuit and System Society

COMMUNITY SERVICE

Guest Editor
- IEEE Access — 2016 – Present

Secretary
- IEEE Tainan Section Circuit and System Chapter — 2014 – Present

Program Committee/Session Chair
- International Conference on Very Large Scale Integration (VLSI-SOC) — 2015, 2016
- Workshop on Compiler Techniques and System Software for High-Performance and Embedded Computer (CTHPC) — 2015
- International Computer Symposium (ICS) — 2010
- International Symposium on VLSI (ISVLSI) — 2012
- Symposium Digital Life Technologies — 2010, 2011
- VLSI Design/CAD Symposium — 2014, 2013, 2012, 2011

Reviewer
- IEEE Transactions on VLSI (TVLSI) — 2015, 2014, 2013
- IEEE Transactions on CAD (TCAD) — 2015, 2014, 2013
- IEEE Transactions on Computer (TC) — 2016, 2015
- IEEE Embedded System Letter (ESL) — 2015, 2013

- Engineering Applications of Artificial Intelligence (EAAI) 2015
- Microprocessor and Microsystem 2015
- Journal of Electrical and Computer Engineering 2015
- Taiwan IEEE Best Paper Award Committee 2015
- Design Automation for Embedded Systems 2015
- Circuits, Systems & Signal Processing 2015
- VLSI Design/CAD Symposium 2015
- Workshop on Compiler Techniques and System Software for High-Performance and Embedded Computer (CTHPC) 2015
- Design Automation Conference (DAC) 2016, 2015, 2014, 2013
- International Conference on Computer-Aided Design 2014
- International Symposium on Circuits and Systems (ISCAS) 2014
- Journal of Information Science and Engineering (JISE) 2014
- International Computer Symposium (ICS) 2014